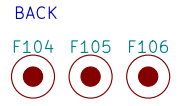
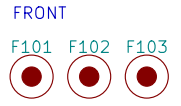
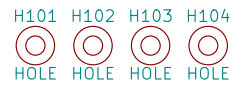
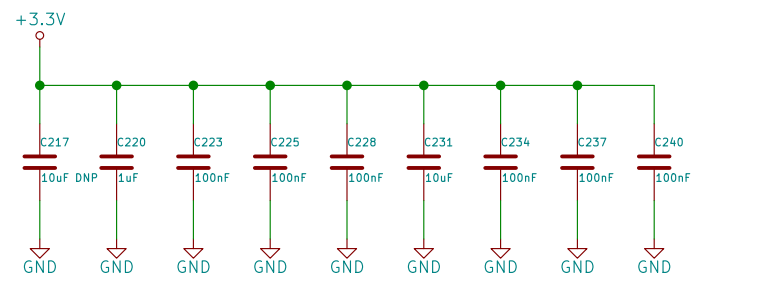
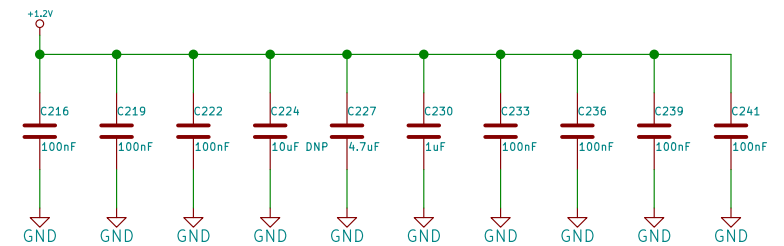
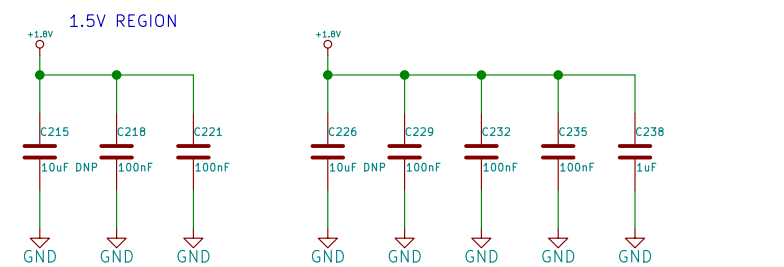
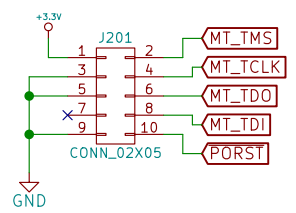
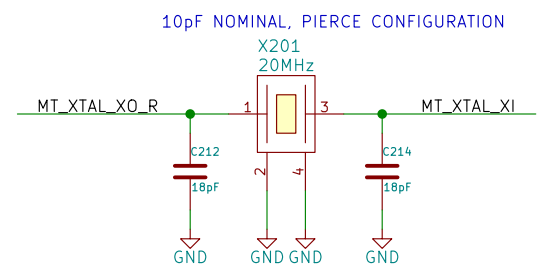
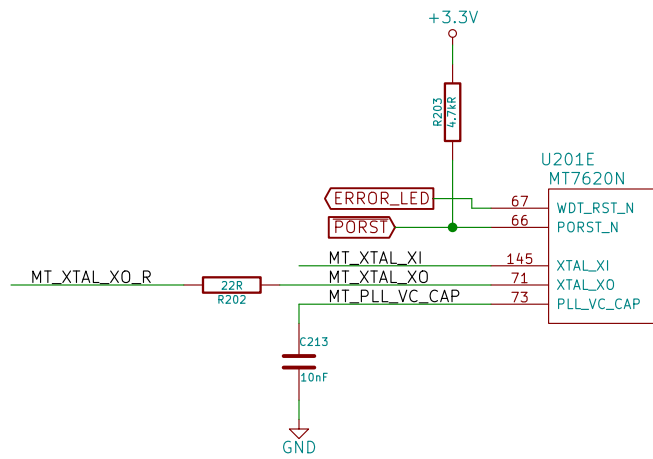
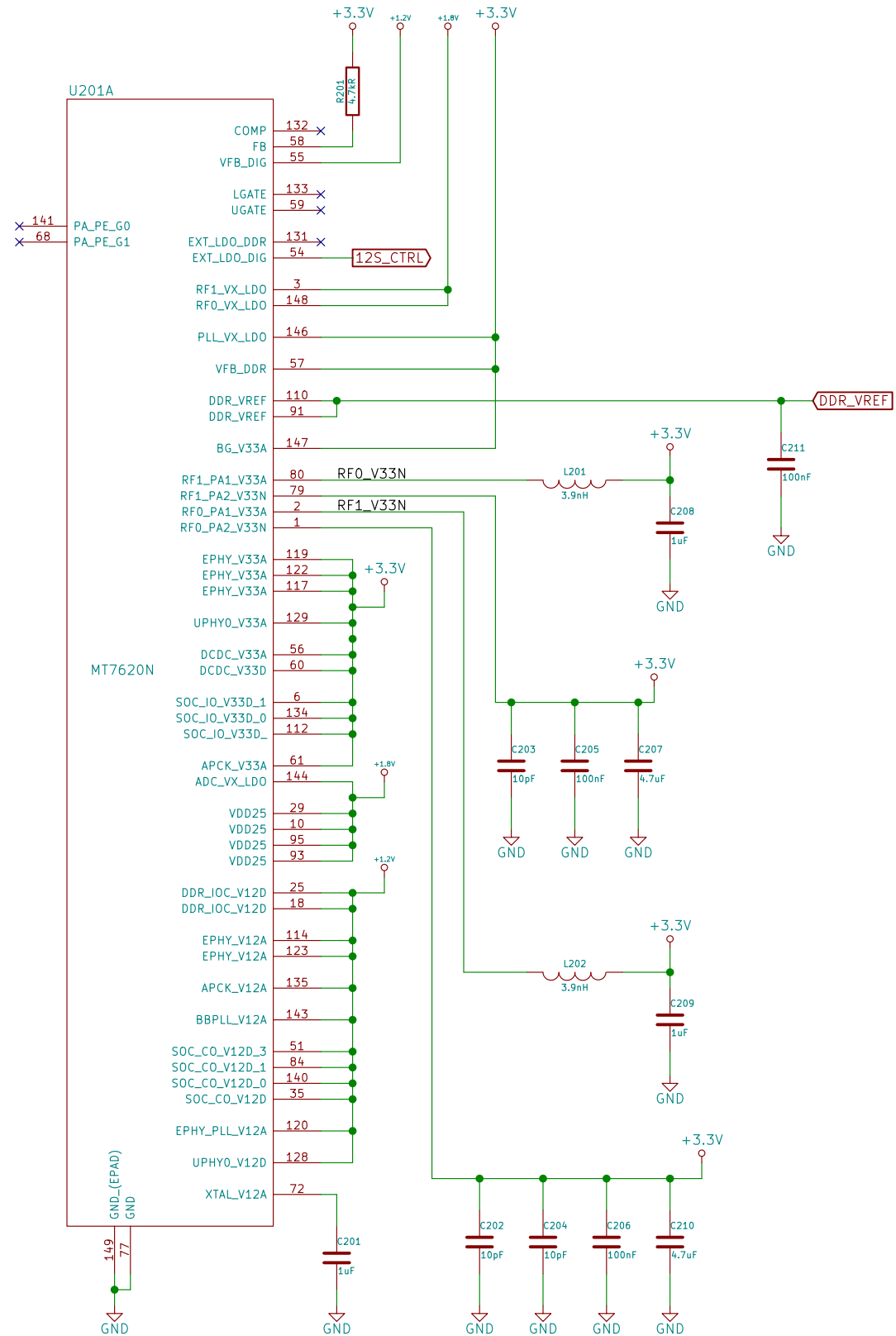


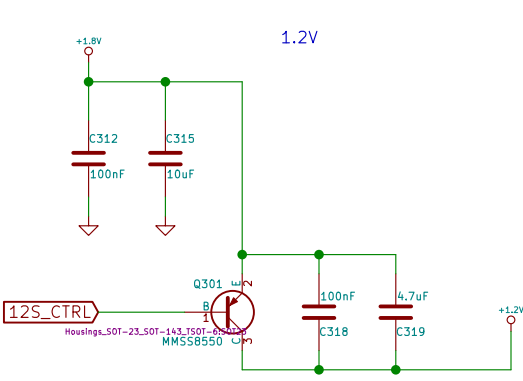
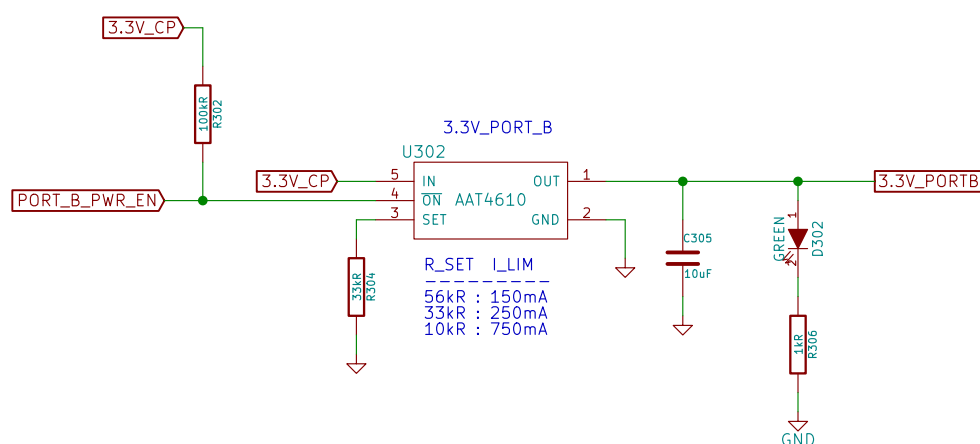
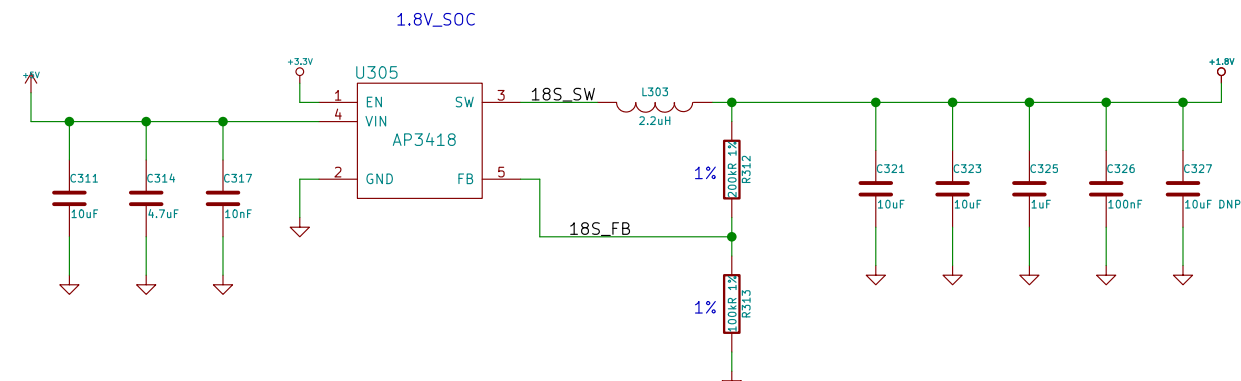
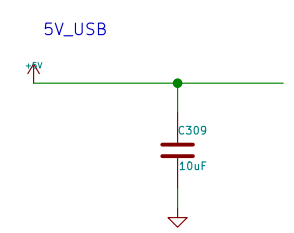
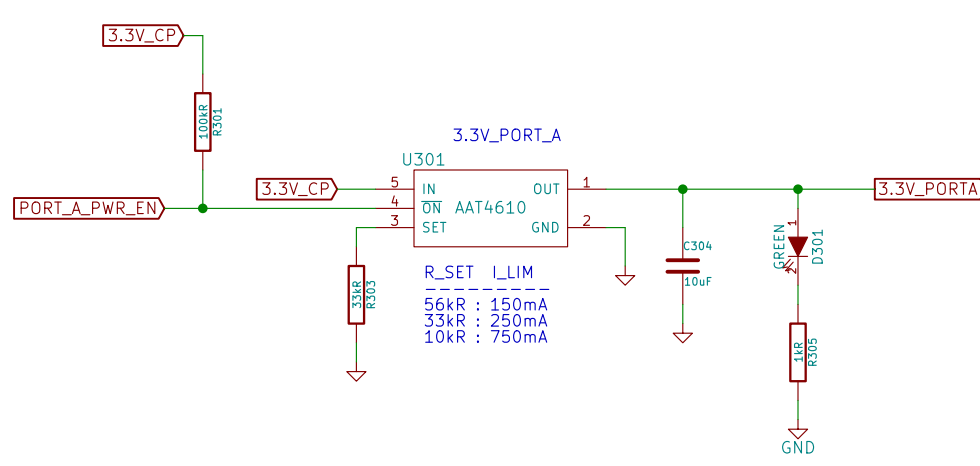
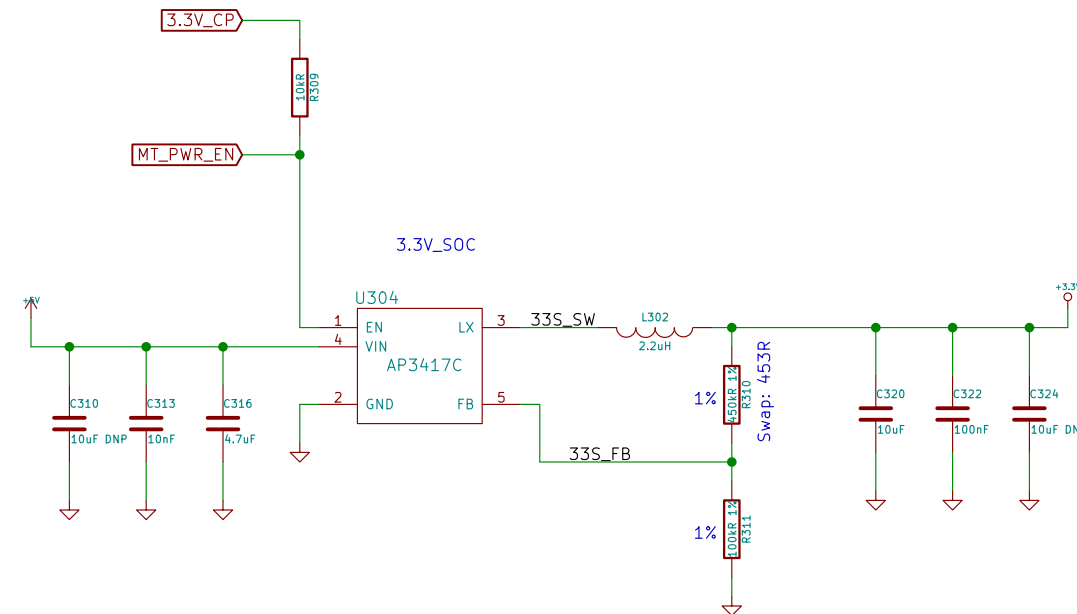
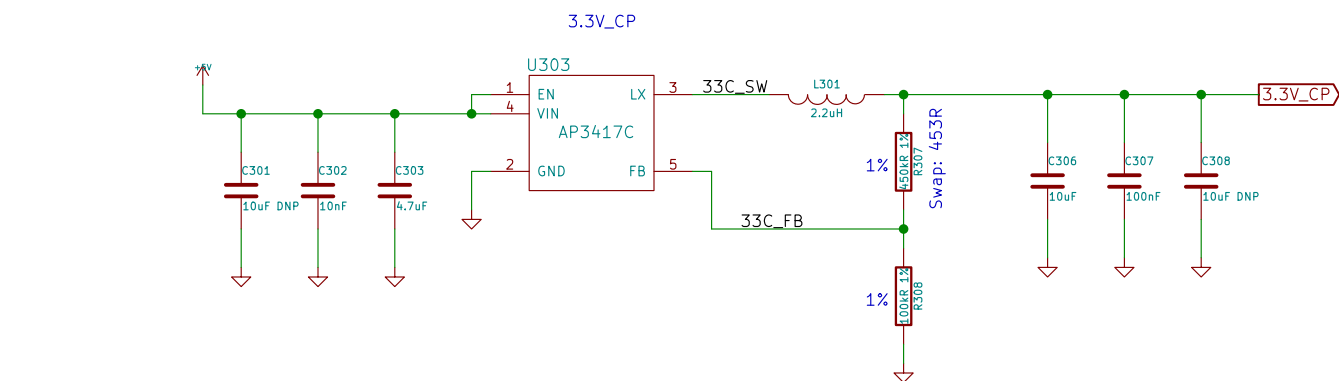
HOLES, LOGOS, AND FIDUCIALS



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<b>Title: Tessel 2 Preliminary Schematic</b>		
Size: B	Date: Wed 04 Mar 2015	Rev: TM-T2-03
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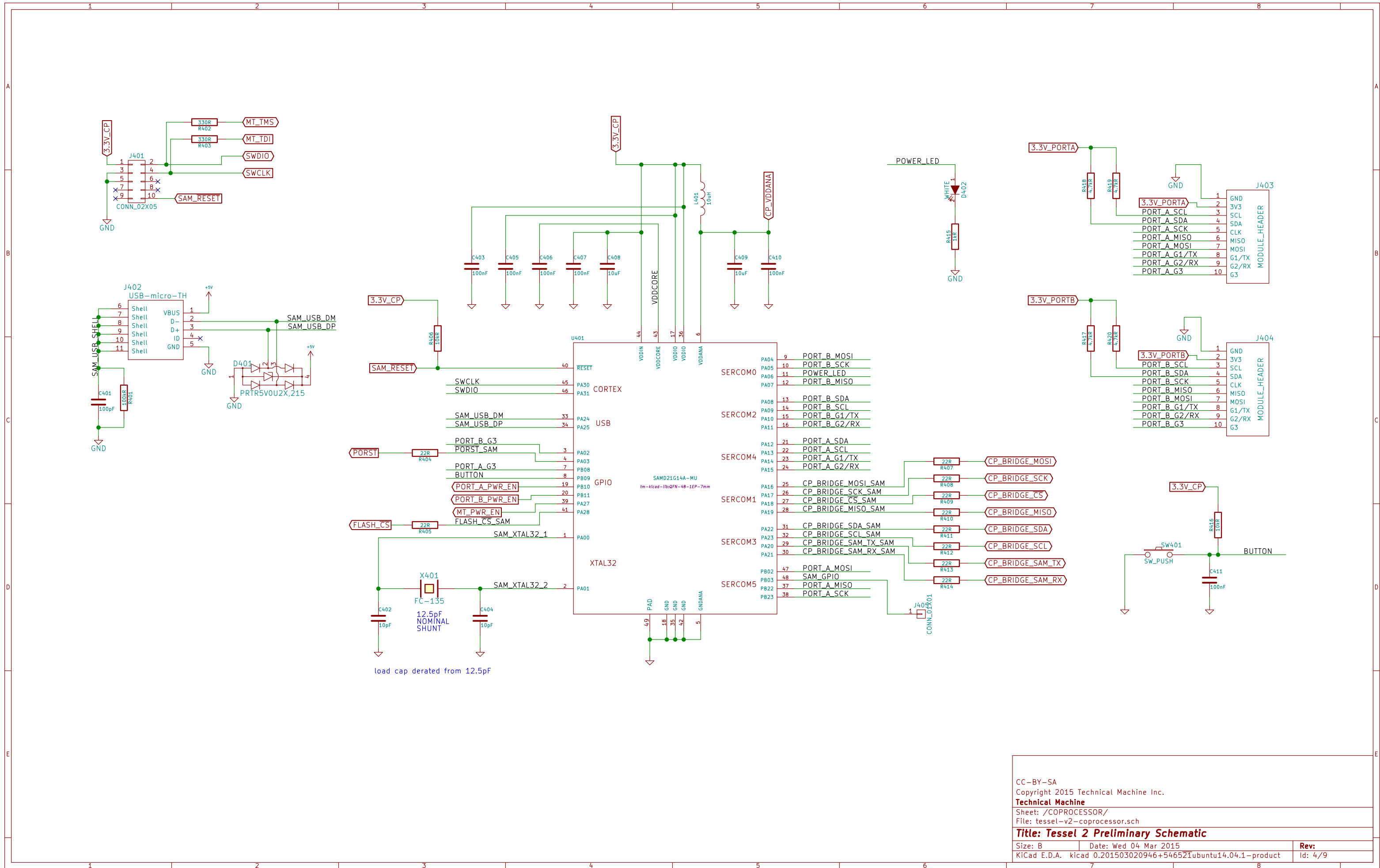


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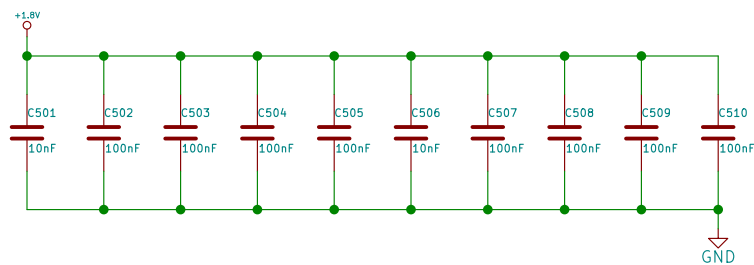
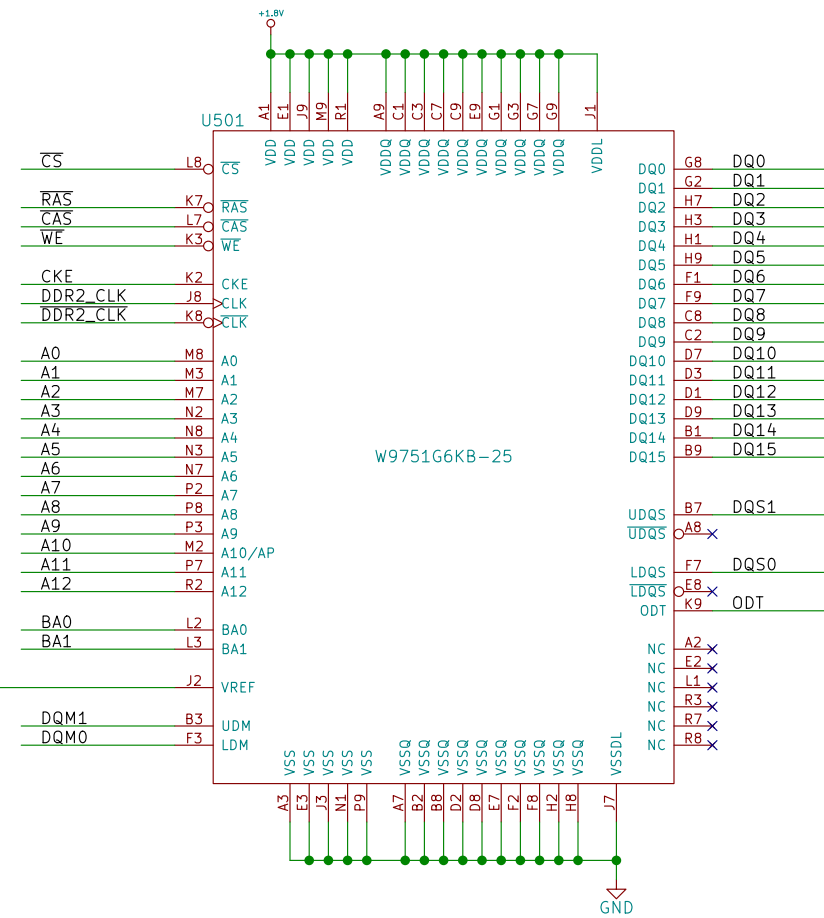
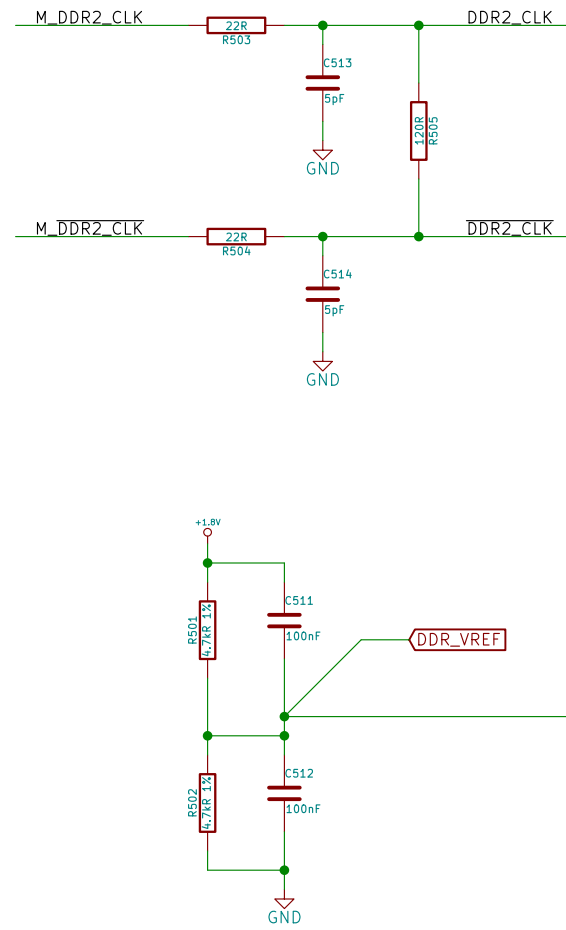
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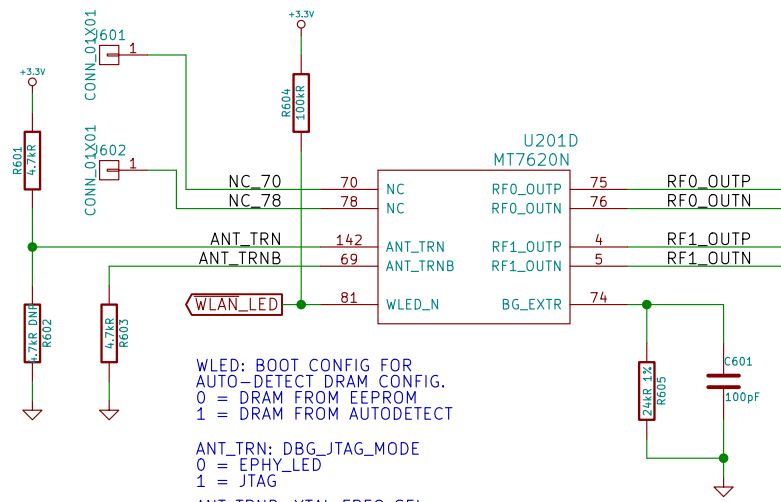
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DQ1	26	DDR_DQ1	DDR_MA1	107	A1
DQ2	99	DDR_DQ2	DDR_MA2	96	A2
DQ3	27	DDR_DQ3	DDR_MA3	31	A3
DQ4	102	DDR_DQ4	DDR_MA4	21	A4
DQ5	23	DDR_DQ5	DDR_MA5	106	A5
DQ6	101	DDR_DQ6	DDR_MA6	97	A6
DQ7	100	DDR_DQ7	DDR_MA7	30	A7
DQ8	88	DDR_DQ8	DDR_MA8	22	A8
DQ9	11	DDR_DQ9	DDR_MA9	104	A9
DQ10	87	DDR_DQ10	DDR_MA10	32	A10
DQ11	12	DDR_DQ11	DDR_MA11	98	A11
DQ12	86	DDR_DQ12	DDR_MA12	105	A12
DQ13	13	DDR_DQ13	DDR_ODT	17	ODT
DQ14	85	DDR_DQ14	MCK_N	16	M_DDR2_CLK
DQ15	14	DDR_DQ15	MCK_P	90	M_DDR2_CLK
DQM0	28	DDR_DQM0	DDR_CKE	34	CKE
DQM1	15	DDR_DQM1	DDR_CS_N	94	CS
DQS0	103	DDR_DQS0	DDR_CAS_N	19	CAS
DQS1	89	DDR_DQS1	DDR_RAS_N	92	RAS
BA0	33	DDR_BA0	DDR_WE_N	109	WE
BA1	108	DDR_BA1			



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**Title: Tessel 2 Preliminary Schematic**

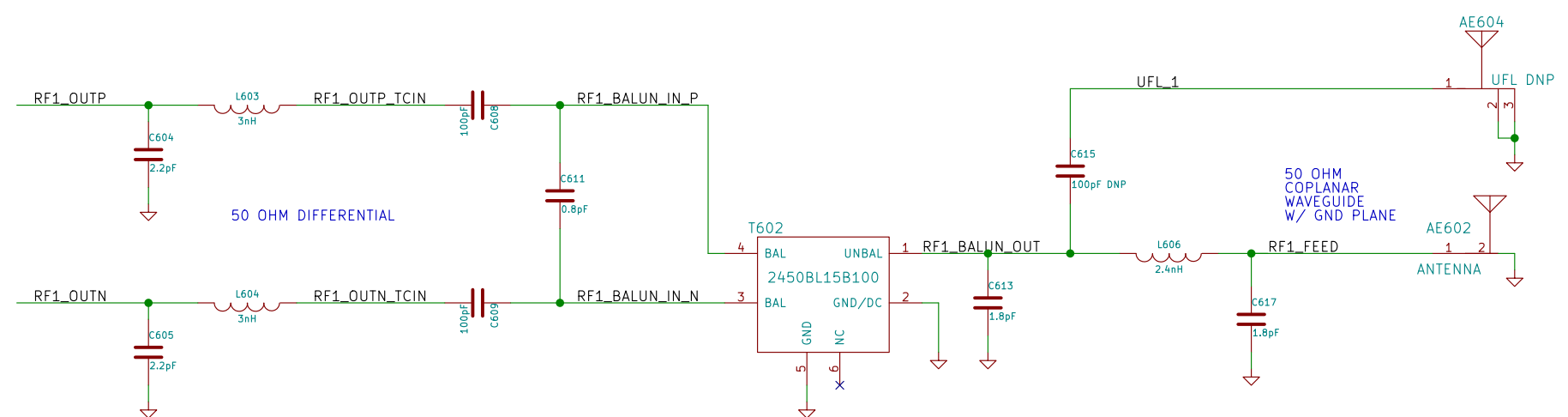
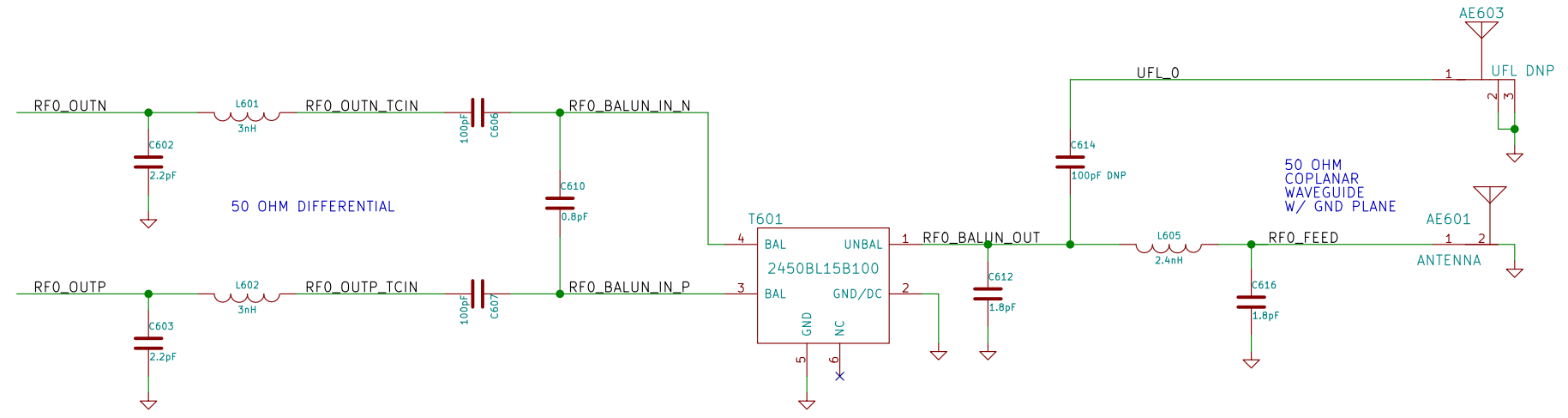
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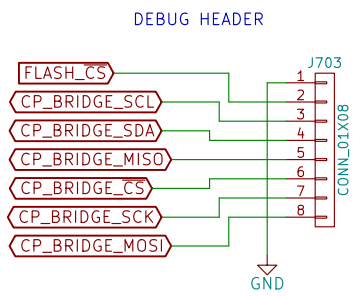
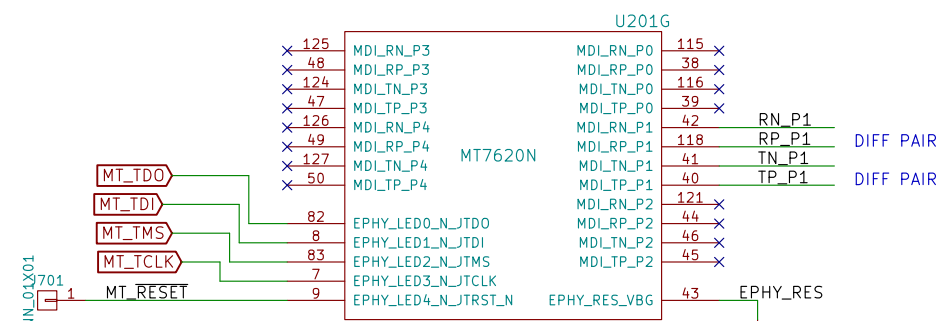
WLED: BOOT CONFIG FOR  
 AUTO-DETECT DRAM CONFIG.  
 0 = DRAM FROM EEPROM  
 1 = DRAM FROM AUTODETECT

ANT\_TRN: DBG\_JTAG\_MODE  
 0 = EPHY\_LED  
 1 = JTAG

ANT\_TRNB: XTAL\_FREQ\_SEL  
 0 = 20MHz  
 1 = 40MHz

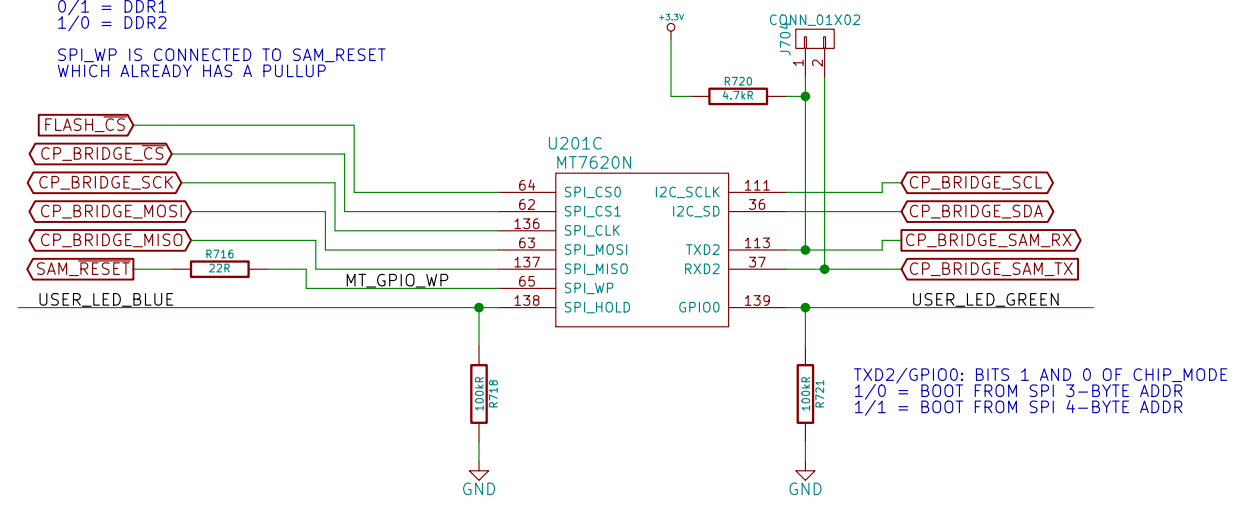


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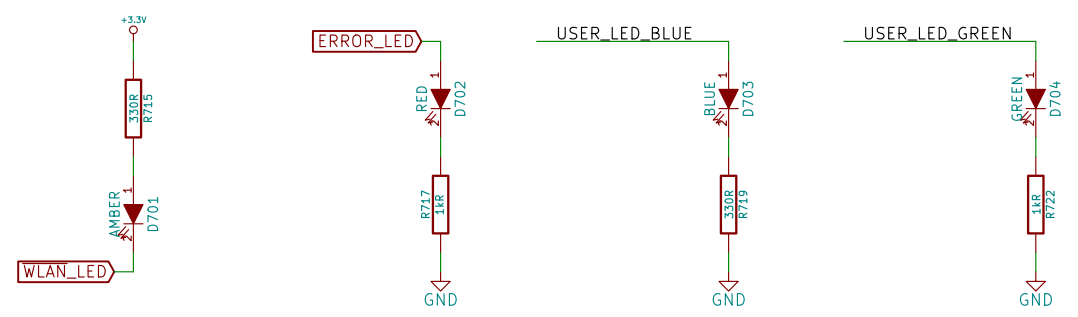
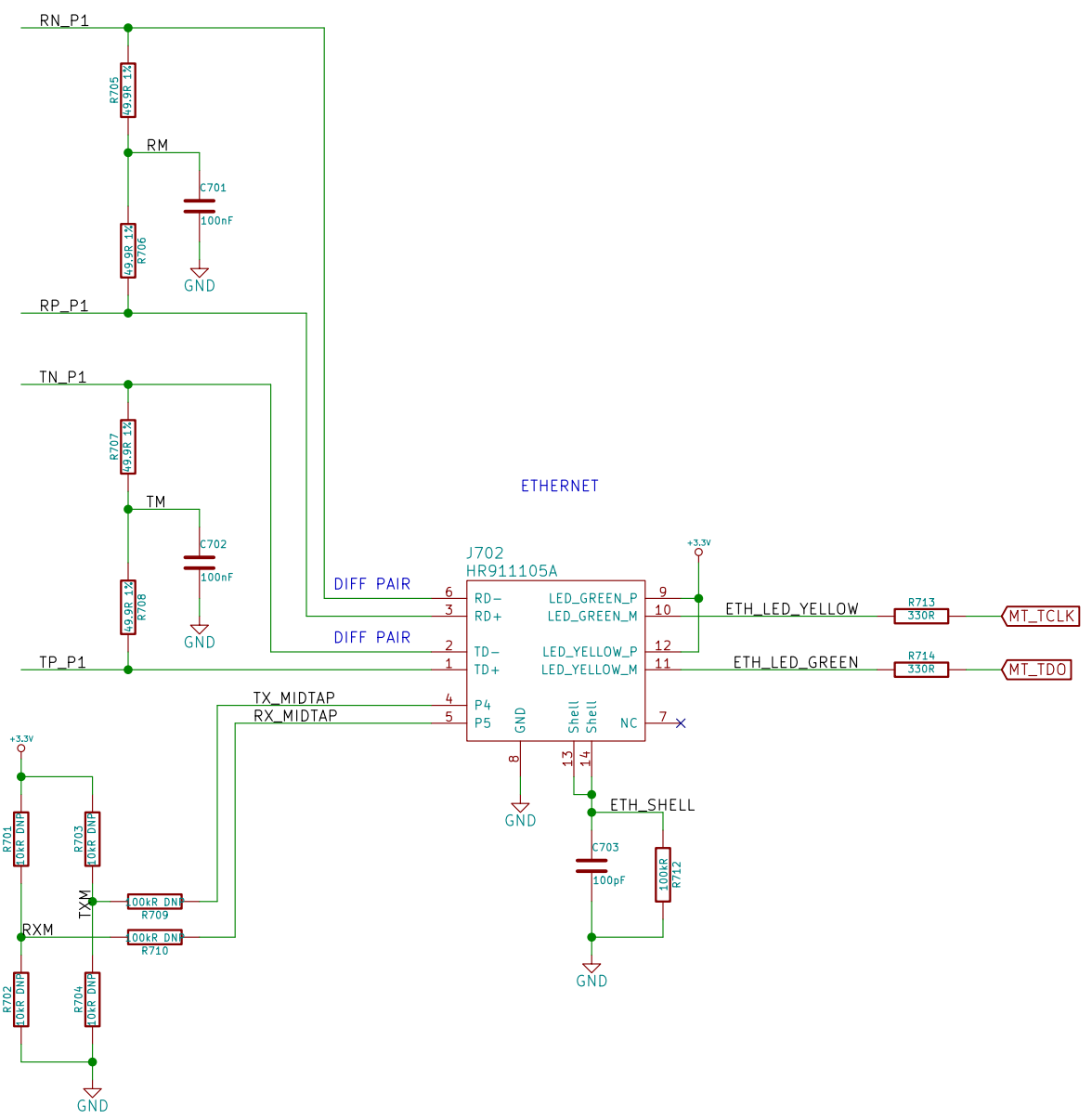


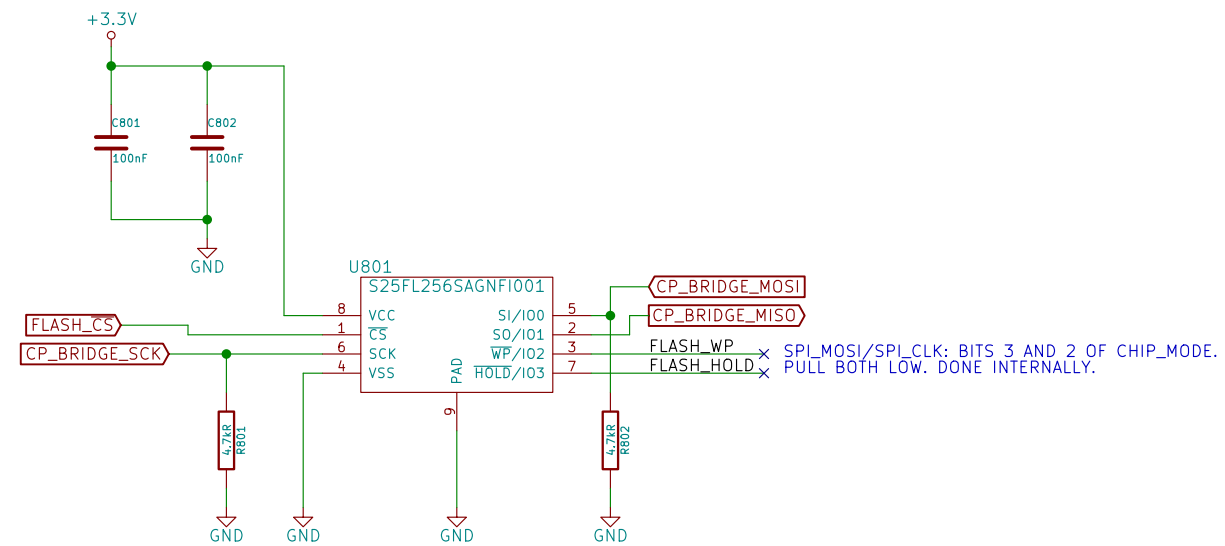
SPI\_WP/SPI\_HOLD: DRAM\_TYPE  
0/0 = SDRAM  
0/1 = DDR1  
1/0 = DDR2

SPI\_WP IS CONNECTED TO SAM\_RESET WHICH ALREADY HAS A PULLUP



TXD2/GPIO0: BITS 1 AND 0 OF CHIP\_MODE  
1/0 = BOOT FROM SPI 3-BYTE ADDR  
1/1 = BOOT FROM SPI 4-BYTE ADDR



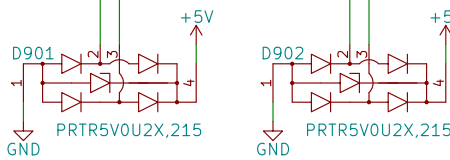
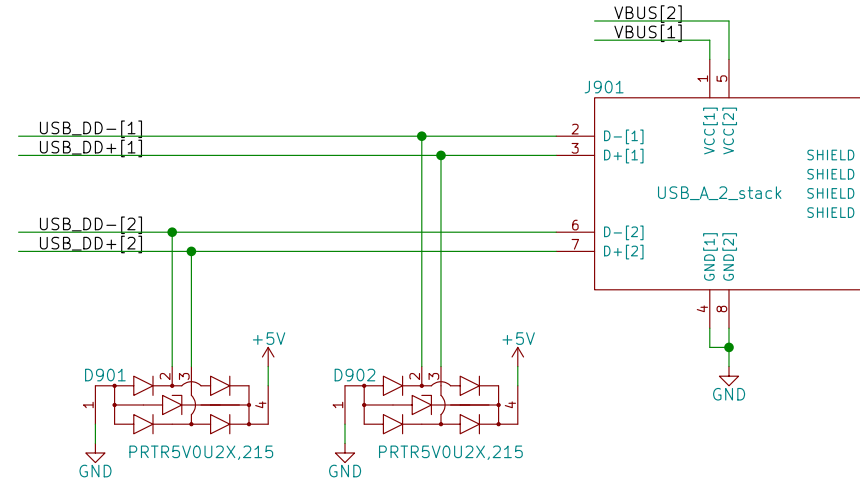
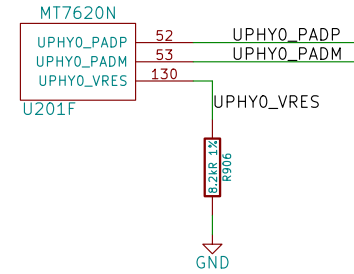
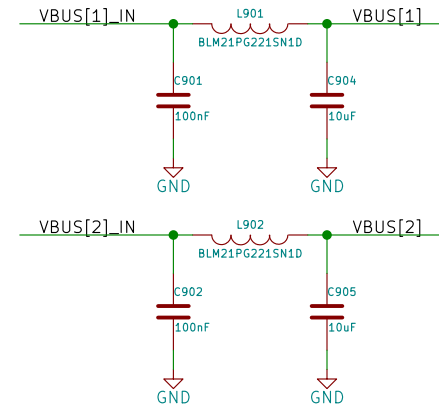
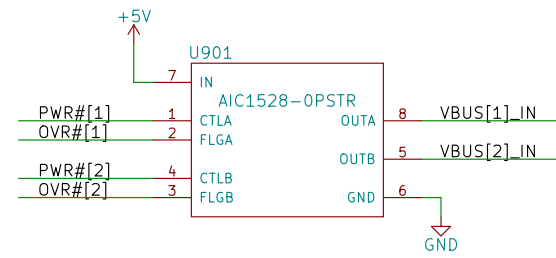


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TWO ADDITIONAL USB PORTS OPTIONAL

